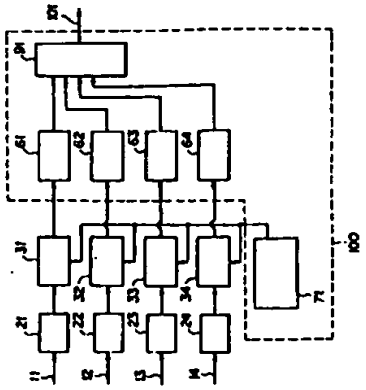
(54) DATA MULTIPLEX TRANSMITTER
(11) 4-242336 (A) (43) 31.8.1992 (19) JP
(21) Appl. No. 3-3522 (22) 17.1.1991
(71) FUJITSU LTD (72) ATSUSHI ENDO
(51) Int. Cl⁵. H04J3/06,H04J3/04

PURPOSE: To realize the data multiplex transmitter employing only one read address control section to reduce the hardware with respect to the data multiplex transmitter multiplexing data inputted plural transmission lines so as not to be overlapped on a same time axis and sending the result.

CONSTITUTION: When a synchronization pattern of a data inputted via transmission lines 11-14 is detected by synchronization detection sections 21-24, memories 31-34 store a data inputted via the relevant transmission lines 11-14, and when the data is stored in all the memories, a read address control section 71 reads the data simultaneously from each memory and inputs the data to delay sections 61-64, a data selection section 91 extracts selectively a data outputted from the delay section 61-64 in the order of the 1st, 2nd and 3rd transmission line···, and the data inputted from the plural transmission lines 11-14 is multiplexed and outputted to a transmission line 101.

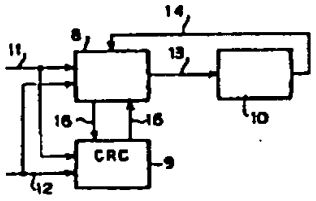


100: read control section

(54) FRAME SYNCHRONIZATION SYSTEM
(11) 4-242337 (A) (43) 31.8.1992 (19) JP
(21) Appl. No. 3-15010 (22) 16.1.1991
(71) MITSUBISHI ELECTRIC CORP (72) KEIJI KURAMASU
(51) Int. Cl⁵. H04L7/08,H04N1/36

PURPOSE: To suppress deterioration in the return characteristic of frame synchronization in the frame synchronization system utilizing CRC.

CONSTITUTION: A reception data storage buffer of a frame synchronization detection section 8 and a latch circuit of a CRC processing section 9 are reset by a reset signal 12. Then the frame synchronization detection section 8 detects a frame synchronization pattern every time one bit of a reception data string is inputted and the CRC processing section 9 calculates a CRC data 15 from a data 16 inputted from the reception data by a multi-frame. Then the CRC check bit in the frame received this time and the arithmetic data having been calculated for each 1-bit input in advance are collated on the condition of the detection of the frame synchronization pattern. Thus, the correctness of the CRC check bit is discriminated as soon as the synchronization pattern is detected.



10: frame synchronization detection timing generating section

(54) ELECTRONIC CONFERENCE PROCESSING SYSTEM
(11) 4-242338 (A) (43) 31.8.1992 (19) JP
(21) Appl. No. 3-15833 (22) 16.1.1991
(71) FUJITSU LTD (72) OSAMU WATANABE
(51) Int. Cl⁵. H04L12/18

PURPOSE: To realize the system to replace a conventional oral conference sufficiently and to attain the efficient operation of the conference with respect to the electronic conference processing system adopting the configuration that a server edits utterance information noticed from a terminal equipment and notifies the result as conference display information to each terminal equipment.

CONSTITUTION: A server is provided with an input analysis section 11 analyzing order of utterance given in noticed utterance information and a name of a speaking party of the utterance and a name of an original speaking party relating to the utterance, a relation decision section 12 deciding the logical relation between utterance information sets corresponding to time series information according to the result of analysis of the input analysis section 11, and a display decision section 13 deciding the display mode of conference display information to be noticed in a way that the logic relation decided by the relation decision section 12 is displayed distinctly, and the relation of significance of the utterance information talked at an oral conference is grasped by displaying the conference display information of the display mode decided by the display decision section 13 onto a terminal equipment.